mined surface area on which to form transistors;

a continuum of uniformly spaced transistors formed in and covering at least a major portion of said predetermined surface area of said semiconductor wafer with said transistors being of substantially identical N-channel and P-channel MOSFET transistors, said transistors defining a configurable gate array from which at least one application specific integrated circuit (ASIC) chip is capable of being formed, said configurable gate array being free of predefined boundaries along which the semiconductor wafer must be cut; and

a plurality of islands in said surface area surrounded by said plurality of transistors, said islands being void of said transistors and occupying a minor portion of said predetermined surface area to define a locale for receiving devices other than said transistors.

8. A master slice configurable gate array for use in the producing of at least two semiconductor chips, each of said semiconductor chips having an area which includes at a base layer level only a plurality of transistors, comprising:

a semiconductor wafer;

said semiconductor wafer having a predetermined surface area on which to form said configurable gate array;

said configurable gate array being formed from a continuum of transistors formed in and substantially covering at least a major portion of said predetermined surface area of said semiconductor wafer and being free of predefined boundaries therebetween;

said transistors being of substantially identical N-channel and P-channel type MOSFET transistors; and

said continuum of transistors defining a region of said predetermined surface area within which said semiconductor chips are formed entirely of said transistors by selectively connecting together a subset of the continuum of transistors and cutting through unconnected transistors to separate the ASIC chip from the wafer.

9. The master slice as defined in claim **8**, wherein a portion of said predetermined surface area comprises:

a vacant peripheral area extending in a band on said predetermined surface area and along an edge of said wafer surrounding said sea of transistors to define a border on said wafer between said wafer edge and said sea of transistors, said vacant peripheral area being void of any of said transistors.

10. The master slice as defined in claim **9**, further comprising:

a plurality of islands in said predetermined surface area surrounded by said continuum of transistors, said islands being void of said transistors and occupying a minor portion of said predetermined surface area to define a locale for receiving devices other than said transistors.

11. The master slice as defined in claim **8**, further comprising:

a plurality of islands in said predetermined surface area surrounded by said continuum of transistors, said islands being void of said transistors and occupying a minor portion of said predetermined surface area to define a locale for receiving devices other than said transistors.

12. The master slice as defined within claim **11** wherein at least one of said islands falls within said region of said predetermined surface.

13. The master slice as defined in claim **11** wherein at least one of said islands falls outside of said region of said predetermined surface.

14. The master slice as defined in claim **11** wherein at least one of said plurality of islands contains an alignment marker.

15. The master slice as defined in claim **11** wherein at least one of said plurality of islands contains test means.

16. The master slice as defined in claim **11** wherein at least one of said plurality of islands contains an application specific integrated circuit.

17. The master slice as defined in claim **8** wherein at least a portion of said continuum of transistors within said region comprises an input to and another portion of said continuum of transistors and an output to the remainder of said continuum transistors within said region.

18. A configurable gate array comprising:

a semiconductor wafer having a major surface;

a continuum of transistors that are uniformly spaced in rows and columns throughout substantially the entire major surface of the wafer, said transistors being free of boundaries therebetween, said wafer containing a sufficient number of transistors to form a variety of application specific integrated circuit (ASIC) chips of different sizes from the same wafer size, the ASIC chips ranging from an ASIC chip of a first size using a first number of transistors to a second ASIC chip of a second size utilizing substantially all of the continuum of transistors in the wafer; and

saw lane channels overlying selected portions of the transistors in the semiconductor wafer, said saw lane channels defining lanes for cutting the wafer through portions of the underlying transistors to define a desired ASIC chip from the wafer.

* * * * *